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Applicant(s) : Edward G. Combs *et al.*

Serial No. : 10/803,782 **Group Art Unit** : TBA

Filed : March 18, 2004 **Examiner** : TBA

For : ***Method of Manufacturing Enhanced Thermal Dissipation Integrated Circuit Package***

I hereby certify that this :

1. Submission of Corrected Specification and Application Papers;;
2. Substitute Specification (15 pages);
3. Original signed page 8 of preliminary amendment previously submitted; and
4. return receipt postcard.

are being deposited with the United States Postal Service via First Class Mail in an envelope addressed to: Commissioner for Patents, PO Box 1450, Alexandria, VA 22313-1450

June 15, 2004

By: Sandina M. Marino
Sandina M. Marino

Milbank, Tweed, Hadley & McCloy LLP
One Chase Manhattan Plaza
New York, New York 10005

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Docket No. 36080.00802

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Serial No.	:	10/803,782	**Group Art Unit**	:	TBA
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SUBMISSION OF CORRECTED SPECIFICATION AND APPLICATION PAPERS

COMMISSIONER FOR PATENTS
Washington, D.C. 20231

Applicants respectfully submit a corrected specification for the above identified application. The application as filed on March 18, 2004 inadvertently had erroneous page numberings in it. Specifically, following page 13, the next page was numbered 17 and the next 19. The enclosed specification has accurate page numbering.

The total pages of this specification is therefore "15" and not "19" as erroneously indicated on the Utility Patent Transmittal, return receipt postcard and Certificate of Mailing by Express Mail. Applicants respectfully submit that no new matter is contained in the enclosed corrected specification and that the only change is the page numbering.

Applicants have also enclosed an original executed page 8 of the Preliminary Amendment that was filed with this application. Mistakenly, the original signature page was not included. Applicants again respectfully submit that no new matter is introduced by this page as it only contains a brief conclusion and fee authorization.

Applicants respectfully submit that no fee is required in connection with this Submission. However, the Commissioner is hereby authorized to charge any

additional fees as may be required or credit any overpayment to Deposit Account No. 13-3250, Order No. 36080-00802.

Respectfully submitted,
MILBANK, TWEED, HADLEY & McCLOY LLP

June 15, 2004

Christopher J. Gaspar
Reg. No. 41,030

Milbank, Tweed, Hadley & McCloy LLP
1 Chase Manhattan Plaza
New York, NY 10005-1413
(212) 530-5000 / (212) 530-5219 (facsimile)

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IN THE UNITED STATES
PATENT AND TRADEMARK OFFICE

U.S. NON-PROVISIONAL PATENT APPLICATION

FOR

METHOD OF MANUFACTURING ENHANCED THERMAL DISSIPATION INTEGRATED CIRCUIT PACKAGE

Inventors:
Edward G. Combs
Robert P. Sheppard
Tai Wai Pun
Hau Wan Ng
Chun Ho Fan
Neil R. McLellan

Milbank, Tweed, Hadley & McCloy, LLP
One Chase Manhattan Plaza
New York, NY 10005

"METHOD OF MANUFACTURING ENHANCED THERMAL DISSIPATION INTEGRATED CIRCUIT PACKAGE"

FIELD OF THE INVENTION

The present invention relates to integrated circuit packaging and manufacturing thereof, and more particularly, to integrated circuit packaging for enhanced dissipation of thermal energy.

BACKGROUND OF THE INVENTION

A semiconductor device generates a great deal of heat during normal operation. As the speed of semiconductors has increased, so too has the amount of heat generated by them. It is desirable to dissipate this heat from an integrated circuit package in an efficient manner.

A heat sink is one type of device used to help dissipate heat from some integrated circuit packages. Various shapes and sizes of heat sink devices have been incorporated onto, into or around integrated circuit packages for improving heat dissipation from the particular integrated circuit package. For example, U.S. Patent No. 5,596,231 to Combs, entitled "High Power Dissipation Plastic Encapsulated Package For Integrated Circuit Die," discloses a selectively coated heat sink attached directly on to the integrated circuit die and to a lead frame for external electrical connections.

SUMMARY OF THE INVENTION

In one aspect, the invention features an integrated circuit package with a semiconductor die electrically connected to a substrate, a heat sink having a portion thereof exposed to the surroundings of the package, a thermally conductive element thermally coupled with and interposed between both the semiconductor die and the heat

sink, wherein the thermally conductive element does not directly contact the semiconductor die, and an encapsulant material encapsulating the thermally conductive element and the heat sink such that a portion of the heat sink is exposed to the surroundings of the package.

In another aspect, the invention features an integrated circuit package with a semiconductor die electrically connected to a substrate, a heat sink having a portion thereof exposed to the surroundings of the package, means for thermally coupling the semiconductor die with the heat sink to dissipate heat from the semiconductor die to the surroundings of the package, wherein the means for thermally coupling is interposed between the semiconductor die and the heat sink but does not directly contact the semiconductor die, and means for encapsulating the thermally conductive element and the heat sink such that a portion of the heat sink is exposed to the surroundings of the package.

In yet another aspect, the invention features an integrated circuit package with a substrate having an upper face with an electrically conductive trace formed thereon and a lower face with a plurality of solder balls electrically connected thereto, wherein the trace and at least one of the plurality of solder balls are electrically connected, a semiconductor die mounted on the upper face of the substrate, wherein the semiconductor die is electrically connected to the trace, a heat sink having a top portion and a plurality of side portions, a thermally conductive element thermally coupled to but not in direct contact with the semiconductor die, wherein the thermally conductive element is substantially shaped as a right rectangular solid, is interposed between said semiconductor die and said heat sink, and is attached to said heat sink, and an

encapsulant material formed to encapsulate the upper face of the substrate, the semiconductor die, the thermally conductive element and substantially all of the heat sink except the top portion and the side portions of the heat sink.

In a further aspect, the invention features an integrated circuit package with a substrate having means for electrically interconnecting a semiconductor die and means for exchanging electrical signals with an outside device, a semiconductor die attached and electrically connected to the substrate by attachment means, a heat sink having means for dissipating thermal energy to the surroundings of the package, means for thermally coupling the semiconductor die to the heat sink to dissipate heat from said semiconductor die to the surroundings of said package, wherein said means for thermally coupling is interposed between said semiconductor die and said heat sink but does not directly contact the semiconductor die, and means for encapsulating said semiconductor die, said thermally conductive element and said heat sink such that said portion of said heat sink is exposed to the surroundings of said package but is substantially encapsulated.

In another aspect, the invention features a method of manufacturing an integrated circuit package including installing a carrier onto an upper surface of a substrate, wherein the carrier defines a cavity, attaching a semiconductor die to the upper surface of the substrate within the cavity of the carrier, aligning an assembly over the semiconductor die, wherein the assembly comprises a heat sink and a thermally conductive element, resting the assembly on the carrier such that the thermally conductive element does not directly contact the semiconductor die, and encapsulating the cavity to form a prepackage such that a portion of the heat sink is exposed to the surroundings of the package.

In yet another aspect, the invention features a method of manufacturing an integrated circuit package including installing a carrier onto a substrate, attaching a semiconductor die to the substrate, aligning an assembly over the semiconductor die, wherein the assembly has a heat sink and a thermally conductive element, resting the assembly on the carrier such that the thermally conductive element does not directly contact the semiconductor die, and encapsulating the thermally conductive element and the heat sink such that a portion of the heat sink is exposed to the surroundings of the package.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing features and other aspects of the invention are explained in the following description taken in connection with the accompanying drawings, wherein:

FIG. 1 is a simplified cross-sectional view of an integrated circuit package according to one embodiment of the present invention;

FIG. 2 is a simplified cross-sectional view of a subassembly of the integrated circuit package shown in FIG. 1, prior to encapsulation and singulation assembly steps;

FIG. 3 is a simplified cross-sectional view of an integrated circuit package according to another embodiment of the invention, which has a direct chip attachment;

FIG. 4A is a plan view of the subassembly of FIG. 2 having one type of heat sink assembly used in the integrated circuit package shown in FIG. 1;

FIG. 4B is a plan view of a subassembly of an integrated circuit package having a second type of heat sink capable of being used in the integrated circuit package shown in FIG. 1;

FIG. 5 is a plan view of the heat sink shown in the subassembly of FIG. 4A;

FIG. 6 is a plan view of a heat sink assembly as shown in FIG. 4A, which becomes the heat sink shown in FIG. 5 once assembled into an integrated circuit package such as the embodiment shown in FIG. 1;

FIG. 7 is a plan view of a third type of heat sink capable of being used in the integrated circuit package shown in FIG. 1;

FIG. 8 is a plan view of a fourth type of heat sink capable of being used in the integrated circuit package shown in FIG. 1;

FIG. 9A is a plan view of a matrix frame containing a "3x3" matrix of heat sinks of the type shown in FIG. 5;

FIG. 9B is a plan view of another matrix frame containing a "2x3" matrix of heat sinks of the type shown in FIG. 4B;

FIG. 10 is a simplified cross-sectional view along line A-A of the heat sink shown in FIG. 5, and a thermally conductive element of one embodiment; and

FIG. 11 shows a flowchart of major steps performed in assembly of one embodiment of an integrated circuit package.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Various embodiments of the integrated circuit package of the present invention will now be described with reference to the drawings.

FIG. 1 shows certain components of an integrated circuit package according to one embodiment of the present invention displayed in their respective positions relative to one another. The integrated circuit package depicted in FIG. 1

generally includes a substrate 100, a heat sink 110, an adapter assembly 120, a semiconductor die 130 and an encapsulant 140. Each of the foregoing will now be described in greater detail along with the manufacturing steps (shown in FIG. 11) associated with them.

A substrate 100 of either a rigid material (*e.g.*, BT, FR4, or ceramic) or a flexible material (*e.g.*, polyimide) has circuit traces 102 onto which a semiconductor die 130 can be interconnected using, for example, wire bonding techniques, direct chip attachment, or tape automated bonding. FIG. 1 shows a semiconductor die 130 connected to the traces 102 of the substrate 100 via a gold thermo-sonic wire bonding technique. In such an embodiment, gold wires 104 interconnect the semiconductor die 130 to the traces of the substrate 100. In another embodiment, shown in FIG. 3, the semiconductor die 130 is connected to the traces 102 via a direct chip attachment technique including solder balls 105. The substrate 100 may be produced in strip form to accommodate standard semiconductor manufacturing equipment and process flows, and may also be configured in a matrix format to accommodate high-density packaging.

In one embodiment, the traces 102 are embedded photolithographically into the substrate 100, and are electrically conductive to provide a circuit connection between the semiconductor die 130 and the substrate 100. Such traces 102 also provide an interconnection between input and output terminals of the semiconductor die 130 and external terminals provided on the package. In particular, the substrate 100 of the embodiment shown in FIG. 1 has a two-layer circuit trace 102 made of copper. A multilayer substrate may also be used in accordance with an embodiment. The substrate 100 shown in FIG. 1 has several vias drilled into it to connect the top and bottom portions

of each circuit trace 102. Such vias are plated with copper to electrically connect the top and bottom portions of each trace 102. The substrate 100 shown in FIG. 1 also has a solder mask 107 on the top and bottom surfaces. The solder mask 107 of one embodiment electrically insulates the substrate and reduces wetting (i.e., reduces wanted flow of solder into the substrate 100.)

As shown in FIG. 1, the external terminals of the package of one embodiment of the present invention include an array of solder balls 106. In such an embodiment, the solder balls 106 function as leads capable of providing power, signal inputs and signal outputs to the semiconductor die 130. Those solder balls are attached to corresponding traces 102 using a reflow soldering process. The solder balls 106 can be made of a variety of materials including lead (Pb) free solder. Such a configuration may be referred to as a type of ball grid array. Absent the solder balls 106, such a configuration may be referred to as a type of LAN grid array.

As shown in FIGS. 1 and 2, the semiconductor die 130 may be mounted or attached to the substrate 100 (step 1115) with an adhesive material 115, such as epoxy. However, as shown in FIG. 3, a solder reflow process or other suitable direct chip attachment technique may also be used as an alternative way to attach the semiconductor die 130 to the substrate 100 (step 1115).

In the embodiment shown in FIG. 1, the heat sink 110 is aligned with and positioned above the top surface of the semiconductor die 130, but not in direct contact with any portion of the semiconductor die 130. The heat sink 110 is preferably made of a thermally conductive material such as copper or copper alloy.

One embodiment of an assembly process for manufacturing an integrated circuit package of the present invention uses a carrier 200 as shown in FIGS. 2, 4A and 4B. FIG. 2 shows, in cross-sectional view, a carrier 200 installed onto the substrate 100. The carrier 200 can be mounted on the substrate 100 by mechanical fastening, adhesive joining or other suitable technique (step 1110). The carrier 200 may have one or more recesses 202 sized to accept support structure 114 of a heat sink assembly (step 1125). In general, the carrier 200 is configured to accept either an individual heat sink assembly (as shown in FIGS. 4A and 4B), or a matrix heat sink assembly 310 containing a number of heat sinks 110 (as shown in FIGS. 9A and 9B) in order to align and install heat sinks 110 of either single semiconductor packages, or arrays of packages manufactured in a matrix configuration. The support structure 114 helps to properly align the heat sink 110 during assembly (step 1120) and, accordingly, may be removed (as discussed below) in whole or in part prior to completion of an integrated circuit package. In one preferred embodiment, however, some portions of the support structure 114 remain in the final integrated circuit package and are exposed to the ambient environment. For example, in the embodiment depicted in FIG. 1, portions of the support structure 114 serve as heat dissipation surfaces.

Further details of the heat sink 110 of a subassembly shown in FIG. 4B include extending fingers 116 of the support structure 114. As shown in plan view by FIG. 4B, the fingers 116 may be sized and shaped to engage matching wells or recesses 202 in the supporting walls of the carrier 200 (step 1125). Such fingers 116 in whole or in part support the heat sink 110 prior to encapsulation (step 1130) and align the heat sink 110 above the semiconductor die 130.

A number of types of heat sinks 110 may be used. FIGS. 4B, 5, 7 and 8 each show a different geometry for a heat sink 110. The heat sink 110 may be sized and configured for use in a specific package arrangement. For example, the heat sink 110 may be sized for incorporation into a package having only a single semiconductor die 130 (see FIG. 1). Alternatively, several heat sinks 110 may be arranged in a matrix configuration 300 to accommodate the assembly of several packages at once. Such a matrix configuration 300 is selected to allow each heat sink 110 of the matrix to be aligned with the corresponding semiconductor die 130 and an underlying matrix package substrate 100. Although a 2x3 and a 3x3 matrix of heat sinks 110 within each matrix heat sink assembly 310 are shown in FIGS. 9A and 9B, a number of matrix combinations and configurations are acceptable. FIG. 9A shows a 3x3 matrix of heat sinks 110, wherein each heat sink 110 has a geometry similar to that of an embodiment shown in FIGS. 4A, 5 and 6. FIG. 9B shows a 2x3 matrix of heat sinks 110, wherein each heat sink 110 has a geometry similar to that of an embodiment shown in FIG. 4B.

In one embodiment, the heat sink 110 has a raised portion 112 protruding above a primary plane of the heat sink 110. As shown in FIG. 10, an exposed surface of the raised portion 112 may be plated with nickel 116, and functions as a heat dissipation interface with the ambient environment. The nickel plating 116 protects the heat sink 110 during environmental testing by resisting oxidation of certain heat sink materials, such as copper. The raised portion 112 can be formed by removing the surrounding portion of the upper surface of the heat sink 110, for example, by etching. In a preferred embodiment, the heat sink 110 is also oxide coated to enhance the adhesion between the

encapsulant material 140 and the heat sink 110. The oxide coating may be achieved or applied by chemical reaction.

The adaptor assembly 120 shown in FIGS. 1 and 2 provides a thermal path between the semiconductor die 130 and the heat sink 110. Such an adaptor assembly 120 includes an adaptor element 122 made of a thermally conductive material (*e.g.*, alumina (Al_2O_3), aluminum nitride, beryllium oxide (BeO), ceramic material, copper, diamond compound, or metal) appropriate for heat transfer between the semiconductor die 130 and the heat sink 110. In one embodiment, the adaptor element 122 is shaped as a right rectangular solid, such that its upper and lower faces have dimensions similar to the upper face of the semiconductor die 130.

One dimension of the adaptor element 122 may be selected to match the area of the upper surface of the semiconductor die 130. The thickness of the adaptor element 122 may also be selected to accommodate size variations of the semiconductor die 130 and the heat sink 110. By reducing the distance between the semiconductor die 130 and the externally exposed heat sink 110, the adaptor assembly 120 reduces the thermal resistance of the die-to-sink interface.

In a preferred embodiment, the distance from the upper surface of the semiconductor die 130 to the adaptor element 122 is minimized to reduce the thermal resistance between the semiconductor die 130 and the heat sink 110. However, to avoid imparting stress to the semiconductor die 130, the adaptor element 122 does not directly contact the semiconductor 130 surface. In a preferred embodiment, the distance between the adaptor element 122 and the semiconductor 130 surface is about five (5) mils or less.

An adhesive layer 119, having both high thermal conductivity and deformability to minimize stress, such as an elastomer, may be used to join the adaptor element 122 to the heat sink 110. In a preferred embodiment, such an adhesive layer 119 is electrically and thermally conductive.

The adaptor assembly 120 may also include a polymeric thermal interface 124 between the semiconductor die 130 and the adaptor element 122 to further minimize the thermal resistance of the die-to-sink interface. In a preferred embodiment, the coefficient of polymeric thermal expansion (CTE) of the thermal interface 124 is similar to that of silicon to minimize stress on the semiconductor die 130. In one embodiment, a thermal interface 124 portion of the adaptor assembly 120 may be attached to the heat sink 110 to reduce the distance from the surface of the semiconductor die 130 to the heat sink 110.

As shown in FIG. 1, the semiconductor die 130, adaptor assembly 120 and a portion of the heat sink 110 are encapsulated to form an integrated circuit package according to one embodiment of the present invention. The encapsulant 140 may be an epoxy based material applied by, for example, either a liquid molding encapsulation process or a transfer molding technique. In one assembly method embodiment of the invention, the encapsulation step 1130 occurs after the carrier 200 is attached to the substrate 100 (step 1110), and the heat sink 110 is installed in the carrier 200 (step 1125). During such an encapsulation step 1130, the cavity 204 of the carrier 200 is filled with encapsulant 140. Solder balls 106 are then attached to the traces 102 of the substrate 100 using a reflow soldering process. After such encapsulation and ball attachment assembly steps, the integrated circuit packages are removed from the strip and singulated into

individual units using a saw singulation or punching technique (step 1135). Upon completion of these assembly steps, the top portion 112 and some portions of the support structure 114 of the heat sink 110 remain exposed to allow heat transfer and dissipation to the ambient environment of the integrated circuit package (see FIG. 1).

Although specific embodiments of the present invention have been shown and described, it is to be understood that there are other embodiments which are equivalent to the described embodiments. Accordingly the invention is not to be limited by the specific illustrated embodiments, but only by the scope of the appended claims.